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IBM CORPORATION- AUSTIN (JVL)
C/O VAN LEEUWEN & VAN LEEUWEN
PO BOX 90609
AUSTIN, TX 78709-0609

EXAMINER	
HASSAN, AURANGZEB	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/697,903
Filing Date: October 30, 2003
Appellant(s): HOFSTEE ET AL.

Joseph T. Van Leeuwen, Reg. No. 44,383
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/13/2007 appealing from the Office action mailed 12/15/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,366,109	Matsushita	4-2002
4,292,668	Miller	9-1981

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita (US Patent Number 6,366,109) in view of Miller et al. (US Patent Number 4,292,668 hereinafter "Miller").

As per claims 8, 15 and 21 Matsushita teaches a method, system and product comprising,

one or more processors (processor, lines 40 – 44);

one or more interface pins (column 1, lines 43 – 45);

an interface controller (element 40, figure 1);

a memory accessible by the processors (memory, element 100, figure 4, column 6, lines 18 – 20);

one or more nonvolatile storage devices accessible by the processors (element 9, auxiliary storage such as hard disc drives, a floppy disc drive, etc, figure 1); and

an interface pin assignment tool for assigning one or more of the interface pins to the interface controller, the interface pin assignment tool including:

means for receiving a first assignment request (signal, element 44, figure 1);

means for identifying one or more of the interface pins that correspond to the first assignment request (address signal, element 46, figure 2); and

means for associating the identified interface pins with the selected interface controller (recognition decoder carries out means for associating, column 6, lines 9 – 23).

Matsushita discloses the I/O controller connected to multiple I/O devices but does not explicitly disclose a system having plurality of interface controllers; a means for selecting a first interface controller from the plurality of interface controllers that correspond to the first assignment request.

Miller analogously teaches a plurality of interface controllers (IOC, elements 206, 208, 210, 212, figure 1); and a means for selecting a first interface controller from the plurality of interface controllers that correspond to the first assignment request (selection of IOC based on selection of peripheral device requesting first assignment, column 14, lines 4 – 24).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify Matsushita with the above teachings of Miller such that it comprises an I/O Controller for an I/O device is needed to function appropriately. One of ordinary skill would have been motivated to make such modification in order to

enable the function for a multitude of peripherals to interface via I/O Controllers and processor (column 7, lines 53 – 67, column 8, lines 1 – 10).

Matsushita modified by the teachings of Miller as applied in claims 8, 15 and 21 above, as per claims 9, 16 and 22 Matsushita teaches a method, system and product wherein the identified interface pins are selected from the group consisting of an input interface pin (physical pin, column 3, lines 27 – 32) and an output interface pin (outputs, column 7, lines 6 – 12).

Matsushita modified by the teachings of Miller as applied in claims 8, 15 and 21 above, as per claims 10, 17 and 23 Matsushita teaches a method, system and product comprising,

receiving a second assignment request, the second assignment request corresponding to the identified interface pins (different semiconductor devices, column 6, lines 58 – 67);

selecting a second interface controller from the plurality of interface controllers that correspond to the second assignment request (unit selecting, column 7, lines 56 – 61); and

re-associating the identified interface pins to the second interface controller (column 7, lines 59 – 61).

As per claims 11, 18 and 24 Matsushita teaches a method, system and product wherein the associating is performed using a look-up table (pin correspondence table, column 1, lines 26 – 34).

Matsushita modified by the teachings of Miller as applied in claims 8, 15 and 21 above, as per claims 12, 19 and 25 Matsushita teaches a method, system and product further comprising:

determining whether there are more interface pins that are not associated with the first interface controller (column 6, lines 45 –52); and

assigning the non-associated interface pins to a second interface controller in response to the determination (inactivated, column 6, lines 53 – 57).

As per claims 13, 20 and 26 Matsushita teaches a method, system and product comprising,

receiving data from the identified interface pins (input signal); and

providing the data to the first interface controller (input signal, element 62, figure 2, column 4, lines 45 – 49).

Matsushita modified by the teachings of Miller as applied in claims 8, 15 and 21 above, as per claims 14 and 27 Miller teaches a method and product wherein the associating is performed at system initialization (system startup/initialization sequence, figure 16).

(10) Response to Argument

Appellant's arguments in the brief filed 11/13/2007 have been fully considered but they are not deemed to be persuasive.

The Appellant argues:

"Matsushita teaches a semiconductor device testing system that, among other shortcomings simply does not teach 'selecting ... [an] interface controller...' nor does Matsushita teach or suggest Applicant's claimed limitations of 'associating the identified interface pins with the selected interface controller.' "

Examiner's response:

The Examiner respectfully disagrees. In response to appellant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The Examiner has explicitly made a 35 USC 103 rejection in which the claim limitations have been rejected by the combination of references wherein Miller is relied upon for a selection of an interface controller.

The Appellant argues:

"The Final Office Action contends that Matsushita teaches Applicant's claimed limitation of 'selecting a first interface controller from a plurality of interface controllers that correspond to the first assignment request' citing Matsushita's multiplexers (104, 106, and 108). ... multiplexers used by Matsushita do not teach anything regarding selecting an 'interface controller from a plurality of interface controllers' "

Examiner's response:

The Examiner respectfully disagrees. The Appellant states that the Examiner has cited Matsushita's multiplexers (104, 106, and 108) for selection purposes, however such a citation was not included in the latest Office Action sent out on 7/5/2006. The Examiner notes that the Appellant's arguments cited on page 7 are verbatim to the arguments presented to the Examiner on 3/30/2006 pages 10 and 11, which pertain to a rejection no longer relied upon by the Examiner. The Examiner had initiated a rejection consisting of the combination of Matsushita and Miller for the claim limitations of selecting an interface controller and had withdrawn the multiplexer selection as of 7/5/2006 and arguments are therefore moot.

The Appellant argues:

The Appellant argues that the *"Final Office Action attempts to combine the teachings of Matsushita with those of Miller and reasons that just because Miller teaches a plurality of interface controllers."*

Examiner's response:

The Examiner respectfully disagrees. In response to applicant's argument that Matsushita does not teach a plurality of interface controllers and Miller is combined because it teaches a plurality of interface controllers, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). The Examiner has cited above motivation to combine the references wherein Matsushita teaches an interface controller associated with an I/O device but does not explicitly disclose a method in which one can be selected from a plurality of controllers which is relied upon in Miller.

The Appellant argues:

Neither Matsushita nor Miller teaches the limitation of selecting an interface controller. *"Miller does not teach any of the selection techniques that are taught and claimed by the Appellants. While Miller selects an interface controller from a plurality of controllers, Miller's selection is not based on an assignment request, where the assignment request is also used to identify interface pins."*

Examiner's response:

The Examiner respectfully disagrees. In response to appellant's arguments against the references individually, one cannot show nonobviousness by attacking references

individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The Examiner has explicitly made a 35 USC 103 rejection in which the claim limitations have been rejected by the combination of references wherein Miller is relied upon for a selection of an interface controller. Matsushita teaches an interface controller and multiple I/O devices and Miller teaches a plurality of interface controllers connected to multiple I/O devices. Selection is based upon Miller and the assignment request is evident in Miller (columns 74 – 77, IOC assignment request) as well as Matsushita (signal 44, figure 1).

The Appellant argues:

In reference to the arguments responded to in the Final Office action the Appellant argues that *"the Examiner states that Matsushita 'already teaches a plurality of I/O devices however does not explicitly mention the fact ... that an interface controller is present.' This is a major problem with the Examiner's rejection. Most of the claim limitations are rejected as being taught by Matsushita. ... In Appellants' independent claims, interface pins are dynamically assigned by (1) receiving an assignment request, (2) identifying interface pins that correspond to the request, (3) selecting an interface controller from a plurality of interface controller that corresponds to the assignment request, and then (4) associating the identified interface pins with the selected interface controller. However, here the Examiner freely admits that the primary reference does not even mention that an interface controller is present."*

Examiner's response:

The Examiner respectfully disagrees. The Examiner has provided ample recitation from Matsushita in the rejection above showing limitations as recited in the claims. Furthermore the Examiner explicitly disclosed that Matsushita teaches an interface controller connected to multiple I/O devices but did not disclose the **selecting** algorithm from a plurality of interface controllers for which Miller was introduced as a secondary reference. The Examiner again notes in response to appellant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Originally in the Non-Final Rejection on 12/30/2005 the Examiner considered Matsushita adequate to reject the claims under 35 USC 102 because the claims recited a very broad interface controller, however in abundance of caution the Examiner issued a second Non-Final Rejection on 7/5/2006 to make sure the interface controller was explicitly covered. The Appellant has argued the references individually and not as a combination.

The Appellant argues:

In reference to Miller the Appellant argues that *"the type of controller being taught by Miller is fundamentally different ... nowhere does Miller teach or suggest 'receiving an ... assignment request,' 'identifying ... interface pins that correspond to the ...*

assignment request,' 'selecting a ... controller ... that corresponds to the assignment request,' nor does Miller teach or suggest 'associating the identified pins ..."

Furthermore Appellant continues to argue that *"Miller simply does not teach 'selecting a first interface controller from the plurality of interface controllers ...' "*

Examiner's response:

The Examiner respectfully disagrees. The Appellant has provided a three tier argument with regards to Miller.

The **first** tier:

is attacking the age of Miller and calling it an *"ancient piece of prior art"*, *"25-year old Miller patent"* and *"the computer system Miller described in his 1981 patent."* The Examiner notes that Miller was provided as an abundance of proof that selecting one interface controller from a plurality is not a novel task and furthermore notes that since the reference is ancient as the Appellant has stated, one of ordinary skill in the art would clearly understand a method in which the selection of an interface controller out of a plurality is made.

Furthermore the Examiner notes other rationale that Matsushita teaches a I/O device processing system including an interface controller (40, figure 1) and connectivity to devices (figures 1 and 2) with pin assignment (figure 3 – 5) and Miller teaches a system in which multiple devices are connected at once and one interface controller is selected (selection of IOC based on selection of peripheral device requesting first assignment, column 14, lines 4 – 24) to provide

functionality for the particular device (IOC, elements 206, 208, 210, 212, figure 1).

All of the component parts of Matsushita and Miller were known at the time of the appellant's claimed invention the only difference is the combination of the known elements in a single testing device thus it would have been obvious to one of ordinary skill in the art to combine all the elements in a single testing device to yield a predictable result of assigning interface requests.

The **second** tier:

is arguing Miller alone. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The **third** tier:

is arguing that Miller does not teach selection of an interface controller. It is unclear to the Examiner how the Appellant has argued on page 8, lines 25 and 26 that *"Miller selects an interface controller from a plurality of controllers ..."* yet now makes a contradictory statement that Miller does not select and interface controller. It is readily apparent to one of ordinary skill in the art that Miller has assignment requests to select an interface controller in order to provide functionality in columns 74 – 77, IOC assignment request. Therefore limitations of selecting an interface controller are taught by the reference.

The Appellant argues:

"No Motivation to Combine the Teachings of Matsushita with Those of Miller. Instead, Impermissible Hindsight Was Used in Rejecting Appellants' Claims."

Examiner's response:

The Examiner respectfully disagrees. Motivation to combine the reference has been provided in the rejection above. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). The Examiner has cited a reference, Matsushita that is connected to a device using an interface controller and further has the capability to connect to multiple devices. The teaching it lacked was to be connected to multiple devices all at once for which a reference Miller was provided. An interface controller is not novel and is adequately described in the reference which has been deemed "ancient" and thus well known to one of ordinary skill in the art.

Furthermore the Examiner notes other rationale that Matsushita teaches a I/O device processing system including an interface controller (40, figure 1) and connectivity

to devices (figures 1 and 2) with pin assignment (figure 3 – 5) and Miller teaches a system in which multiple devices are connected at once and one interface controller is selected (selection of IOC based on selection of peripheral device requesting first assignment, column 14, lines 4 – 24) to provide functionality for the particular device (IOC, elements 206, 208, 210, 212, figure 1).

All of the component parts of Matsushita and Miller were known at the time of the appellant's claimed invention the only difference is the combination of the known elements in a single testing device thus it would have been obvious to one of ordinary skill in the art to combine all the elements in a single testing device to yield a predictable result of assigning interface requests.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Aurangzeb Hassan
Patent Examiner
Art Unit 2182

Conferees:

/Lynne H Browne/
Lynne H. Browne
Appeal Practice Specialist, TQAS
Technology Center 2100

Henry W. H. Tsai
TC2100 Supervisory Patent Examiner
Art Unit 2184